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Design of Low Power Digitally Operated Voltage Regulator by using CMOS Technology

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Abstract: As portable electronic devices become a part of daily life, it creates a huge market for electronic components for those battery driven devices. Low-power digitally operated (LPDO) voltage regulator is an important part that provides steady DC supplies for other components. Low power, low noise and high stability are the desired features of a regulator. Here, A Low-Power Digitally Operated (LPDO) Voltage Regulator that can operate with a very small Input-output Differential Voltage with 32nm CMOS technology has been proposed. It increases the Packing Density and provides the new approach towards power management. A voltage regulator is capable of providing 0.8V output under the supply voltage of 1.2V and the output voltage level is controlled externally by means of 2 1-bit control signals.

Keywords: Low Drop-Out, Voltage Regulator, Power management, Reduction in chip Area.

I. INTRODUCTION

A programmable voltage regulator has become an essential part of portable electronic devices, where low power dissipation, low noise and high stability are desired characteristics.

Voltage regulators can be divided into two main categories: Linear Voltage Regulators (LVR) and Switching Mode Power Converters (SMPC). SMPC is restricted in the use of portable electronic devices, because of the high cost, possible electromagnetic interference (EMI), high output voltage ripple and noise . On the other hand, LVR exhibits characteristics of very small output voltage ripple, compactness, and low output noise. Low power digitally operated Voltage (LPDO) Regulator presents the lowest dropout voltage and the highest power efficiency of all the LVR. LPDO is used in battery-powered electronics, where minimum noise is an important issue. However, frequency response of the LPDO system highly depends on load conditions.

In this, a low power, low programmable, low dropout regulator capable of providing 0.8V output has been proposed. Low power digitally operated voltage regulators are the circuit, design to provide a specified stable DC voltage, with low input to output voltage difference. Dropout voltage of regulator is the value of differential voltage at which regulation provided by control loop stops. The low drop out voltage regulator is programmable device and output voltage is controlled externally by means of 2 1- bit controlled signals. The entire circuit has been design in 32nm CMOS technology and simulated using microwind 3.1 tool.

II. LITERATURE REVIEW

From the rigorous review of related work and published literature, it is observed that many researchers have designed Low Power Digitally Operated Voltage Regulator by applying different techniques.

Gabriel Alfonso Rincon-Mora and Philip E. Allen,[1] was studied and designed a low drop out voltage regulators, and published a paper. This paper discusses the important issues related to the design of a LDO circuits. An increasing number of low voltage applications which require the use of LDOs, i.e, cellular phones, pagers, laptops, etc.

R. Jacob Baker, Stuart K. Tewksbury and Joe E. Brewer,[2] had worked on CMOS Circuit Design, Layout and Simulation. In this paper, to encompass both the long- and short-channel CMOS technologies, a two-path approach to custom CMOS integrated circuit design is adopted.

Vincent Lixiang Bu[3] had worked on a CMOS Capacitor less Low Drop-Out Voltage Regulator. In this paper, a 3-5V 50mA CMOS low Drop-out (LDO) linear regulator with a single compensation capacitor of 1pF is presented. The circuit realization is well-studied and developed with respect to the loop-gain response, the transient response, the output noise, the output accuracy, as well as the standby power consumption. The proposed LDO regulator is implemented in the AMI 0.6um CMOS process, the active layout area is 541 x 320 µm.

Robert J. Milliken, Jose Silva-Martínez,[4] had studied and presented a paper on Full On-Chip CMOS Low Drop Voltage Regulator. This paper proposes a solution to the present bulky external capacitor low-dropout (LDO) voltage regulators with an external capacitor less LDO architecture. The large external capacitor used in typical LDOs is removed allowing for greater power system integration for system-on-chip (SoC) applications.

Xinquan Lai And Donglai Xu[5] had studied An Improved CMOS Error Amplifier Design for LDO Regulators in Communication Applications. In this paper, A new CMOS error amplifier, which is primarily used in LDO regulators for communication applications, was presented.

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III . PROBLEM DEFINITION

Conventional LDO Block Diagram

Low-drop out regulators is one of the most conventional applications of operational amplifiers. Figure2 shows the basic topology. A voltage reference is used with the op-amp to generate a regulated voltage Vreg.

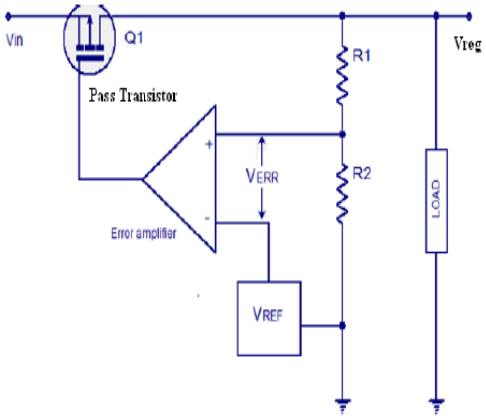

Fig : Conventional LDO

Today, for a battery powered electronics devices, power consumption is become an important parameter. Hence, in order to overcome this problem, LPDO voltage regulator is proposed.

IV. PROPOSED WORK

In this architecture, low power digitally operated voltage regulator capable of providing 0.8v output at the output end has been proposed. in this, a current-sourcing PMOS in the output stage has been introduced. It is required that the PMOS be pulled all the way to ground so as to be biased further into saturation region. For this reason, the existing topology is modified and a common source stage is added. The common-source stage is responsible for enhancing signal swing and boosting. The two gate inputs provided to the proposed LPDO architecture will make the device programmable. Two bit binary values are given to the gate inputs. The variation of the output with respect to these inputs will be as depicted in the following table.

BINARY INPUT	OUTPUT VOLTAGE (V)
00	0.7v to 0.8v
01	0.6v to 0.7v
10	0.6v to 0.7v
11	0.8v

Table : Variation in input and output

The proposed architecture consists of the following stages:
1. Error Amplifier
2. Common Source Amplifier
3. Current-sourcing PMOS

1. ERROR AMPLIFIER

A high gain operational amplifier is used as the error amplifier, with a stable voltage reference fed to one of its input. The voltage reference is usually derived from a band gap reference circuit.

2. COMMON-SOURCE AMPLIFIER

In general, a source follower is used as the buffer stage in most LPDO's. The source follower has asymmetric current driving capability, and gain less than one. Hence a common-source amplifier is used, which has a small signal gain equal to

$$Av=gm(ro1\| ro2)$$

where gm is the transconductance of the amplifying device, ro1 and ro2 are the output resistances of the load and the amplifying device.

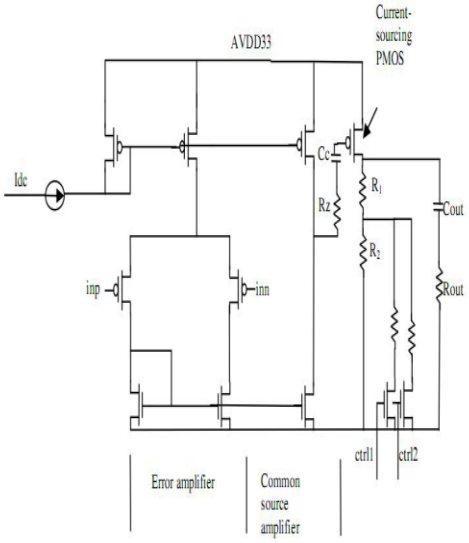

Fig : Schematic of proposed regulator

3. CURRENT-SOURCING PMOS

The sizing of the current-sourcing PMOS is the most vital part of the entire design. PFETs are known to have poor current driving capability, as a result of which a large-size PMOS is required. In our design, a PMOS with high voltage threshold has been used, because Low-voltage threshold FETs are known to contribute to leakage currents, increasing power dissipation in the device. The PMOS is responsible for quick charging and discharging of the output.

V. CONCLUSION

In this paper, we are going to design a low power low drop-out voltage regulator by using 32nm CMOS technology. And the output voltage is control externally by using 2 1-bit control signals. The circuit is capable of providing the output up to 0.88 volts when power supply is at 90% of the desired value, hence the power management is proposed. This LPDO is going to design by using MICROWIND 3.1 tool.

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